REMARKS

In response to the final Office Action mailed April 5, 2007, Applicant respectfully requests reconsideration. Claims 1, 3-15 and 17-23 were previously pending in this application. By this amendment, claim 14 has been amended. No claims have been canceled and no claims have been added. As a result, claims 1, 3-15 and 17-23 are pending for examination with claims 1 and 14 being independent.

I. Rejections Under 35 U.S.C. §103

Claims 1, 3-5, 7, 10, 12-15, 17, 18 and 21 are rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Mahalingaiah (US Patent No. 5,960,467) in view of Gandhi (U.S. Patent No. 6,405,305) and in further view of Meier (US Patent No. 6,405,305). Applicant respectfully traverses this rejection. While Applicant does not believe the combination of Mahalingaiah, Gandhi and Meier is proper, Applicant believes the claims as currently presented distinguish over the combination and therefore will not argue the appropriateness of the combination herein. However, Applicant reserves the right to argue that the combination is improper at a later time if deemed necessary.

The final Office Action concedes that the combination of Mahlingaiah and Gandhi fails to disclose the result of the speculative registers once they become committed to an architectural state. However, the Office Action asserts that "Meier discloses using pointers and renaming schemes to allow a speculative register to become architectural." (Page 4 of the Office Action). However, even if Meier does disclose a pointer renaming scheme to label a speculative register as an architectural register, this disclosure does not anticipate the claims as currently presented. In particular, the claims recite storing a speculative data address for each stage in the pipeline in addition to storing at least one architectural data address.

For example, claim 1 recites "a speculative register file capable of simultaneously storing at least a speculative data address for each of the plurality of pipeline stages and at least one architectural data address, the speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the instruction pipeline and at least one speculative data address after the at least one speculative data address becomes a respective architectural data address." That is, the speculative register file can hold a speculative data

address for each stage, plus an additional architectural data address while still storing a speculative data address for each pipeline stage.

Meier does not disclose maintaining a speculative data address for each pipeline stage, even after committing one or more data addresses to architectural data addresses. Rather, Meier discloses converting one of the speculative registers into an architectural state. This technique actually reduces the number of speculative registers available for storing speculative data address. Meier is completely silent with respect to providing a speculative register file having a speculative register for each stage in the pipeline and a speculative register to store one or more additional architectural addresses. As conceded by the Office Action, Mahalingaiah and Gandhi fail to disclose this limitation and therefore do not cure this deficiency.

Accordingly, the combination of Mahalingaiah, Gandhi and Meier does not disclose or suggest a digital signal processor having "a speculative register file capable of simultaneously storing at least a speculative data address for each of the plurality of pipeline stages and at least one architectural data address, the speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the instruction pipeline and at least one speculative data address after the at least one speculative data address becomes a respective architectural data address," as recited in claim 1. Therefore, claim 1 patentably distinguishes over the combination and is in allowable condition.

Claims 3-13 depend from claim 1 and are allowable based at least on their dependency.

Claim 14, as amended, recites a method for operating a digital signal processor, comprising generating speculative data addresses in response to address operands and one or more address parameters, executing an instruction using data at a location specified by the speculative data addresses in a pipelined execution unit having a plurality of stages, holding speculative data addresses in a speculative register file as a corresponding instruction advances through the pipeline, the speculative register file capable of storing a speculative data address for each of the plurality of stages in the pipelined execution unit and at least one architectural data address, holding one or more speculative data addresses that have become architectural data addresses in the speculative register file, and writing the speculative data address to the speculative register file as the speculative data address is generated by the address generator.

The combination of Mahalingaiah, Gandhi and Meier nowhere discloses or suggests "holding speculative data addresses in a speculative register file as a corresponding instruction advances through the pipeline, the speculative register file capable of storing a speculative data address for each of the plurality of stages in the pipelined execution unit and at least one architectural data address," as recited in claim 14. Therefore, claim 14 patentably distinguishes over the combination and is in allowable condition.

Claims 15 and 17-23 depend from claim 14 and are allowable based at least on their dependency.

In view of the foregoing, Applicant respectfully requests that the rejection under 35 U.S.C. §103 be withdrawn.

III. Final Rejection

While the claims have been finally rejected, Applicant respectfully points out that independent claim 1, for which the Examiner has already performed a search, has not been amended herein. Moreover, claim 14 was amended to recite a register file with the capacity to store a speculative data address for each stage in the pipeline and at least one architectural address, similar to the limitation recited in claim 1. Therefore, the amendment to claim 14 does not raise any new issues or require further searching. Accordingly, Applicant respectfully requests that the amendments after final be entered and the arguments presented herein fully considered.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: July 5, 2007

Respectfully submitted,

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